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RESEARCH ARTICLE

# Energy Shaping Control of Grid Connected Parallel Interleaved Converter for Current Reduction

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## ABSTRACT

This paper implements to control a circulating current with low frequencies produced by parallel interleaved converters. The magnetically linked inductors are used for inverters to parallelize in this configuration. The harmonic content in the output voltage is minimized by incorporating carrier interleaving. This consequences in a greater circulating current to flow in the course of the two Voltage Source Converters (VSCs).The mutual inductance of the Coupled Inductors (CI) is competently reduce the components of circulating currents with high frequencies. The components of low frequencies effectively cannot filter by coupled inductors. The coupled inductors are lead to saturation when the circulating currents are very high under uncontrolled due to this the converter have the higher switching losses, and disgrace the overall performances. The delivered active as well as reactive powers to the grid are effectively controlled with this controller and also it decreases the amount of circulating current with the low frequency. The performances of the converter are found by simulation and compared with the performance of Linear Quadratic (LQ) control and classical PI control. The simulation shows a good performance in the proposed method.

**Key Words**: Voltage Source Inverter, Coupled Inductor, Port Controlled Hamiltonian, Linear Quadratic Control, Proportional Controller, Pulse Width Modulation

## INTRODUCTION

The converters have been a lot of pioneering configurations were incorporated to manage the escalating power received from non conventional sources of energy. For such applications, multi-pulse converters, matrix converters and multi-level converters were offered in [1]. Another topology was projected recently based on the parallelization of typical two-level inverters to attain high power converters by coupled inductors [2, 3]. The various offers offered by parallelized inverters are phase shifted by 180◦ to the system; the benefits are size declined of the output filter, multilevel output, and also reduction of Common Mode Voltage in [4, 5]. The acceptable level of circulating currents with lofty frequency components can be shortened by a tolerable choice of coupled inductors in [6]. In [7] proposed the various design procedures of these filtering components. In [8] proposed a reduction of circulating current in the system and common mode voltage by three-level SVM. The PWM techniques were proposed in [9] to diminish the crest value of the circulating current by discriminating harmonic elimination. The PI controllers inputs are identified from the circulating currents from each phase were presented in [10].

The modulating signals added to controller output of only one converter of the two parallelized VSCs and the proposed scheme of modified DPWM were presented in [11]. In [12], the deadbeat control approaches were implemented in order to reduce the amount of circulating currents. The ZSCC was suppressed by a modular two-level interleaved converter with carrier Phase Shifted PWM was presented in [13]. The ES control strategy was implemented in DFIG wind turbine has been presented in [14].

### CONTROL METHODOLOGY

The scheme of method for the system MMC with VCM as shown in Fig. 1, it consists of five controllers. The five controllers and their control objectives are: (i) a VSI two–layer controller is used to transfer the amount of power generated into the ac grid, (ii) a leg energy controller is used to control the amount of capacitors energy stored in the SMs in order to make sure the stable operation of the MMC, (iii) a phase - disposition pulse width modulation (PD-PWM) type modulator is used to determines the SMs that need to be switched ON and a voltage balancing algorithm (VBA) to balance the capacitors voltage of the SMs, (iv) a amount of circulating current suppressing controller to suppress the inner circulating currents (v) a VCM controller to reimburse for the difference of voltage during unbalance conditions and both the VCM controller and circulating current suppressing controller are decoupled from the main power stage control. The fig. 2 shows the two layers of VSI controller is wrecked into three blocks: (i) power–to–current transformation (ii) a Phase Locked Loop for synchronization of AC grid and (iii) the conventional control of current in the rotating reference frame of direct quadrature to transfer the amount of power generated into the side of AC grid at an random power factor.

#### Phase Locked Loop

The synthesizing the information of phase and frequency of the system by using the technique of PLL. The PLL computes the grid phase angle by sensing the grid voltage and projecting the corresponding space vector onto the dq axis. The q component is then forced to be equal to zero ($v_q = 0$) with the help of a PI controller as depicted in fig. 2. By doing so, the dq axis will be rotating at the same speed as the grid angular frequency. This angle is then used to synchronize the dq reference frame for the control of inner current of the system.

#### Power to Current Transformation

The active power and reactive power references ($P_{ref}$ , $Q_{ref}$) are reliant on the load requirement. From dq currents be able to be computed accordingly and this equation is based on the assumption that the PLL is capable to force $V_q$ to zero.

$$P_{ref} = \frac{3}{2} v_d I_d^{ref} \quad (1)$$

$$Q_{ref} = -\frac{3}{2} v_d I_d^{ref} \quad (2)$$

**Inner Current Control**

The AC side dynamics of the VSI can be described by the following dynamic phasor relation in the 'abc' reference frame, $m_j$, $v_j$ and $i_j$ are the three phase AC voltages and currents at the AC terminal respectively, $L_s$ and $R_s$ are the equivalent value of the inductance and the resistance at the VSI side which are defined by the following equations,

$$L_s \frac{di_j}{dt} = -R_s i_j + V_j - v_j \quad (3)$$

$$L_s = L_f + \frac{L_a}{2} \quad (4)$$

$$R_s = \frac{R_a}{2} \quad (5)$$

**FLY – BACK CONVERTER**

During the operation it has different configuration of Fly-back converter.. From the Fig. 3, the winding of primary of the transformer gets connected when the switch 'S' is 'ON', the input supply with its positive side is connected to the dotted end. The secondary winding connected in series with diode 'D' gets reversed due to the voltage induced in the secondary at the same time. The winding in the primary is able to carry current when turning 'ON' switch 'S', but it blocked the current in the secondary side winding due to the diode reverse biased. This mode of circuit have been denoted here as operation of Mode-1. Fig. (a) Shows the circuit which is current carrying part and Fig. (b) Shows the fly-back circuit during mode-1. The discontinuous flux mode of operation is preferred for enhancing the output voltage. On the other hand, the additional output power can be transferred during continuous mode. The circuit is designed based upon thumb rule for operation of continuous flux mode at the minimum predictable input voltage and at the value of rated output power.

## RESULTS AND DISCUSSIONS

The simulation results corresponding to a proposed converter technique is presented and the simulation can be carried out through MATLAB. Fig. 4 depicts that the three phase voltage in the grid side. Fig. 5 shows the current in the grid side. The Fig. 6 depicts the active power of the converter.

## CONCLUSION

The coupled inductors can be used to interconnect the conventional two-level inverters in parallel for improvement of rated power of converters connected with grid. The balance of the current delivered by the two converters is feasible without any specific control function of the system. At the same time, it induces disagreeable circulating currents with low frequency which stress on power semi-conductors was increases. In this work, magnetically coupled inductors with interleaved three-phase inverters can be balanced by the proposed technique. The converter is considered as a passive system and it was modeled that meets the requirements of energy shaping control. It required additional sensors to implementation of this algorithm to measure the output currents of the first converter. Consequently the projected control allows enhanced performances and abridged energy losses.

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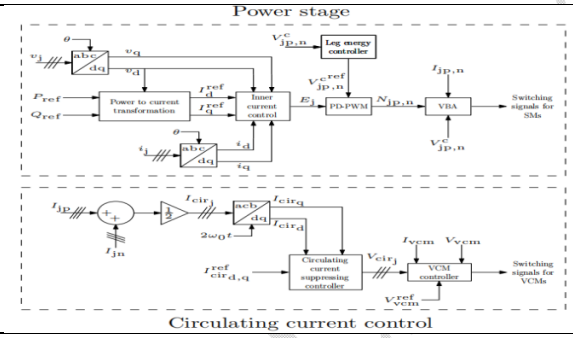


**Fig. 1: Overview of the Overall Control System**

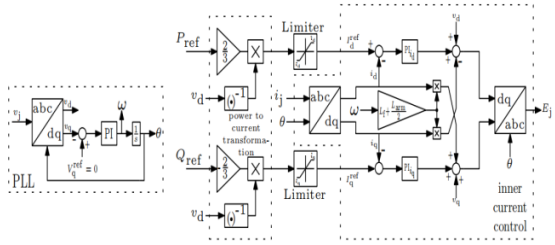


**Fig. 2: Schematic of PLL Controller with two–layer MMC+VCM VSI**

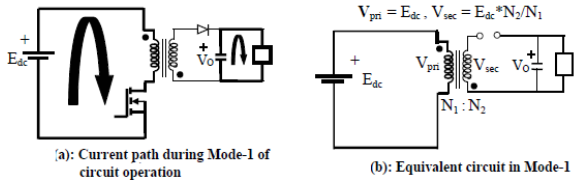


**Fig. 3: Fly- Back Converter during Mode-1 Operation**

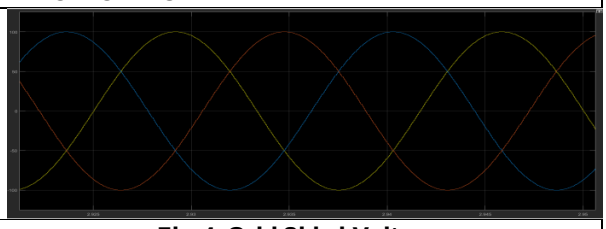

**Fig. 4: Grid Sided Voltage**

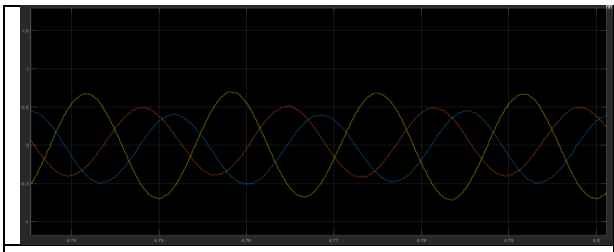

**Fig. 5: Grid Sided Current**

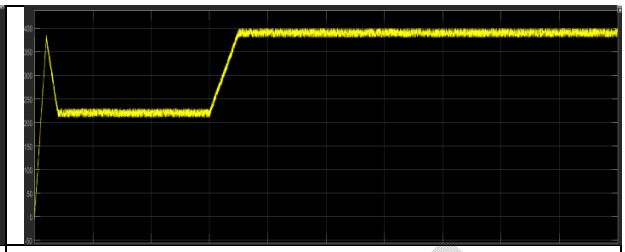

**Fig. 6: Active Power**

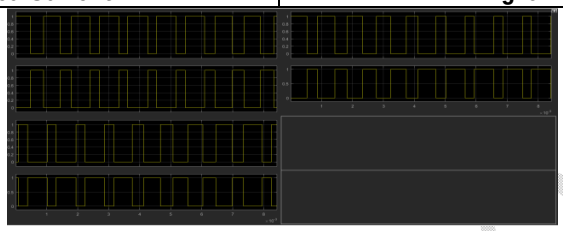

**Fig. 7: Gate Pulse**